REMARKS

In response to the Office Action dated August 31, 2010, Applicant requests consideration of the following remarks. Claims 5, 8, 16, and 18-21 were previously cancelled. Claims 1-4, 6, 7, 9-15, 17, and 22 are currently pending in the application.

I. Claim Rejections - 35 U.S.C. § 103

Rejection of Claims 1-4, 6-7, 9-15, 17, and 22:

Claims 1-4, 6-7, 9-15, 17, and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Publication No. 2002/0176489 to Sririam et al. (herein "Sririam") in view of U.S. Patent No. 6,108,693 to Tamura (herein "Tamura"), U.S. Patent No. 6,928,575 to Okabayashi et al. (herein "Okabayashi"), and U.S. Patent Publication No. 2003/0009772 to Karr (herein "Karr"). Applicant respectfully traverses this rejection.

Sririam discloses a vector correlator based Rake receiver that employs a circular buffer (para. [0007]). Two of the three buffers are available for processing by a correlator datapath while the remaining buffer is being written into by incoming chips (para. 0009]). The triple data buffer implements a sliding buffer of 16-chips in which the buffer slides by an interval of 16-chips in a circular fashion in each iteration (FIG. 1 and para. 0040]). At each correlator co-processor (CCP) iteration, 32-chips from the 48-chip triple data input buffer 100 are available for processing by the CCP datapath. At the next iteration, a new set of 16-chips, along with an older set of 16-chips, becomes available to the datapath (FIG. 1 and para. [0040]).

Tamura discloses a system and method of data communication between processors in a multiprocessor system that includes a transmitting processor, a receiving processor, and a shared memory (col. 2, lines 14-18). Two communication buffers are defined in the shared memory, and the transmitting buffer includes communication buffer selecting means for selecting one of the two communication buffers, and write inhibit means for changing the selected communication buffer to a write-disabled state in order to inhibit writing of the selected communication buffer by other processors (col. 2, lines 19-25). The receiving processor includes communication buffer selecting means for selecting one of the two communication buffers, and read wait means for causing the receiving processor to wait until the selected communication buffer attains a read-enabled state (col. 2, lines 33-40). During

the time that the transmitting processor is writing part of a message to a communication buffer, the receiving processor, even though it is capable of reception, cannot read in the message until writing is finished (col. 1, lines 50-58). However, the communication buffer selecting means of the transmitting buffer writes data by alternately selecting first and second communication buffers, and the buffer selecting means of the receiving processor reads in data by alternately selecting the first and second communication buffers (col. 2, lines 46-55).

Okabayashi discloses an LSI chip 100 on which a first processor 110, a second processor 120, a memory 130, a clock supply unit 140, and a reset control unit 150 all are integrated (Abstract; FIG. 1). The first processor 110 and second processor 120 operate synchronously with first and second internal clock signals ICLK1, ICLK2, respectively, which are generated by the clock supply unit 140 (FIG. 1; col. 3, lines 49-65). The reset control unit 150 supplies reset signals IRES1, IRES2, IRES3 to the clock supply unit 140, the first processor 110, and the second processor 120, respectively, in order to reset each of these system components (FIG. 1; col. 4, lines 6-13). The reset control unit 150 asserts IRES1, IRES2, and IRES3 based on the states of external reset signals, ERES1, ERES2, ERES3, which are input to reset control unit 150 (FIG. 1; col. 4, lines 18-20).

When one of the processors 110, 120 has completed its processing, the external reset signals are asserted to cause the reset control unit 150 to assert the corresponding internal reset signal, IRES2 or IRES3, which will cause the processor to reset (col. 5, lines 14-23). In addition, when one of the processors 110, 120 has completed its processing, clock supply unit 140 may terminate its internal clock signal (i.e., either ICLK1 or ICLK 2), thus reducing power dissipation (col. 6, lines 18-21).

Karr discloses a recording receiver, which receives a transmitted signal, converts the received signal to a digital base-band signal, and stores the digitized base-band signal in a buffer for subsequent processing (Abstract; ¶ [0040]). More specifically, "after a complete transmission sequence is received, the digital data may be later reassembled into the information by a digital signal processor" (¶ [0040]). The digital processor (FIG. 3) uses the output of a crystal oscillator as a clock signal (¶ [0047]). Because the digital data is only processed after a complete transmission is stored in the buffer, the clock signals utilized for signal processing do not need to operate while the receiver is still receiving data from a

particular transmission, and the clock signals used in the signal processor can be disabled during the receive mode (¶ [0047]).

Applicant's claims 1, 9, 10, 13, 17, and 22 (from which the remaining rejected claims depend) include at least the following features, which differentiate claims 1-4, 6-7, 9-15, 17, and 22 from that which is disclosed by Sririam, Tamura, Okabayashi, Karr or their combination (only claim 1 is excerpted below for brevity, as claims 9, 10, 13, 17, and 22 include similarly distinguishing features):

Claim 1:

". . . processing . . . the first digital samples in the first buffer and the second buffer for all known paths of the first group of symbols during a first symbol group duration, wherein the processor is clocked by a processor clock at a clock rate that is faster than and not synchronous with the sample rate;

disabling the processor upon completion of processing the first digital samples by gating off the processor clock, wherein the processor remains disabled through a remainder of the first symbol group duration;

simultaneously with processing the first digital samples, buffering second digital samples corresponding to a second group of symbols into the second buffer and a third buffer, . . . wherein the first symbol group duration represents a duration of time during which the second digital samples are buffered into the second buffer and the third buffer;

at a beginning of a second symbol group duration that occurs consecutively with an end of the first symbol group duration, enabling the processor to process the second digital samples . . ."

Neither Sririam, Tamura, Okabayashi, Karr nor their combination disclose each and every feature of claims 1-4, 6-7, 9-15, 17, and 22. Applicant's claims 1, 9, 10, 13, 17, and 22 are distinguishable from the cited references for the following reasons:

A) None of the cited references disclose a triggering event for gating off the processor clock, which is completion of processing a set of digital samples, as is claimed by Applicant. The Office Action states that Sririam does not disclose the idea of a processor/component disabling upon the completion of a task or process, and relies on Tamura as disclosing this feature of Applicant's claims (Office Action, page 6). Applicant agrees that Sririam does not disclose this feature, but traverses the assertion that Tamura does disclose this feature.

The cited portion of Tamura (col. 2, lines 56-67, see Office Action, page 7) that the Office Action asserts to disclose this feature states the following:

> Preferably, the shared memory has, for each of the two communication buffers, a status flag for controlling write and read enable/disable of the communication buffer; the initial state of the status flag being write-enabled and read-disabled. The write inhibit means of the processor on the transmitting side sets the status flag of the selected communication buffer from write-enabled to write-disabled. The write-completion notifying means sets the status flag of the selected communication buffer from read-disabled to read-enabled. The read completion notifying means of the processor on the receiving side sets the status flag from write-disabled to write-enabled.

Applicant asserts that, not only does the cited portion of Tamura fail to disclose the feature of "disabling the processor upon completion of processing the first digital samples," but that Tamura specifically states the opposite. First, Tamura is directed to write-enabling/read-disabling a communication buffer, and is not directed toward enabling or disabling a processor. The argument in the Office Action seems to be avoiding this distinction by stating that "Tamura discloses the idea of processor/component disabling upon the completion of a task or process" (Office Action, page 6). In other words, the argument lumps together processor/component as if they are interchangeable or that the enabling/disabling that occurs in Tamura is somehow generically applicable to a buffer AND a processor. It is not. The enabling/disabling discussed in Tamura relates to write-enabling/read-disabling a communication buffer. This concept of write-enabling/read-disabling is not relevant to a processor, and therefore it is fallacious to say that the disclosure in Tamura of write-enabling/read-disabling a communication buffer is analogous to disabling

a processor. Further, write-enabling/read-disabling a communication buffer does not actually involve "disabling" the communication buffer, but merely involves disabling a certain functionality of the communication buffer (e.g., reading from the buffer). The converse functionality (e.g., writing to the buffer) is enabled at times when the buffer is read-disabled, and therefore the communication buffer is not actually "disabled" in a complete sense.

Second, in Tamura, the "processor" necessarily needs to remain enabled, because it is the processor that controls the setting of the status flag associated with write-enabling/read-disabling the communication buffer. Accordingly, Tamura actually teaches away from the concept of disabling a processor, since that would destroy the ability of the system (e.g., the processor) to toggle the write-enable/read-disable flag for the communication buffer. For at least these reasons, Applicant asserts that Tamura is insufficient to disclose the feature of "disabling the processor upon completion of processing the first digital samples . . . through a remainder of the first symbol group duration," as is asserted in the Office Action (page 6).

B) None of the cited references disclose a system in which enabling the processor clock is triggered by completion of buffering a next set of digital samples and the occurrence of a beginning of a next symbol group, as is claimed by Applicant. As discussed above, Applicant disagrees that Tamura discloses the feature of "disabling the processor upon completion of processing the first digital samples . . . through a remainder of the first symbol group duration," as is asserted in the Office Action (page 6). Applicant further asserts that none of the references disclose that a triggering event for enabling the processor is completion of buffering a next set of digital samples AND the occurrence of a beginning of a next symbol group duration.

The Office Action relies on Okabayashi as disclosing the feature of "after completion of buffering the second digital samples and at a beginning of a second symbol group duration . . . enabling the processor to process the second digital samples" (Office Action, page 8). Applicant traverses the assertion that Okabayashi does disclose this feature.

The cited portion of Okabayashi (col. 5, lines 14-23, see Office Action, page 8) that the Office Action asserts to disclose this feature states the following:

> Where one of the processors **110** and **120** has completed its processing or where it is needed to have one of the processors **110** and **120** restart its processing from the beginning, ERES**2** or ERES**3** may be asserted. For example, where the second processor **120** has completed its processing, ERES**3** may be asserted. In this case, since the reset control unit **150** asserts only IRES**3**, only the second processor **120** is reset. This is to say, the first processor **110**, memory **130** and clock supply unit **140** continue their operations without being suspended.

Applicant asserts that, although the cited portion of Okabayashi discuss restarting a processor "where it is needed", Okabayashi and the other references fail to disclose that the triggering event for enabling the processor clock is completion of buffering a next set of digital samples AND the occurrence of a beginning of a next symbol group duration. This combination of triggering events is simply not disclosed in any of the cited references.

C) None of the cited references disclose a system in which buffering the digital samples from the receiver is capable of occurring BOTH while the processor is processing digital samples AND while the processor is disabled, as is claimed by Applicant. The Office Action states that the combination of Sririam, Tamura, and Okabayashi do not disclose the idea where digital samples from a receiver can be buffered while the processor is disabled, and relies on Karr as disclosing this feature of Applicant's claims (Office Action, page 9). Applicant agrees that Sririam, Tamura, and Okabayashi do not disclose this feature, but traverses the assertion that Karr is an appropriate reference to be used to disclose this feature.

The cited portion of Karr (¶ [0047], see Office Action, page 10) that the Office Action asserts to disclose this feature states the following:

> [**0047**] The output of the oscillator is utilized as the local oscillator (LO) for the receiver illustrated in **FIG. 3**. The digital processor illustrated in **FIG. 3** utilizes the output of the crystal oscillator as a clock signal. As stated previously with respect to **FIG. 3**, the digital data is only processed after a complete transmission is stored in the buffer (i.e., "recorded"). Thus, the clock signals utilized for signal processing do not need to operate while the receiver is still receiving data from a particular transmission. By "recording" data during a receive mode and "processing" the data subsequently (e.g., a processing mode), the clock signals used in the signal processor can be disabled such that the overall noise level in the receiver during the critical reception time period can be greatly reduced.

Karr also states the following:

> [**0040**] In operation, information is modulated on a carrier signal and transmitted into free space (not shown). The antenna in the recording receiver system (**300**) is tuned to the carrier signal and produces a received signal. The receiver demodulates the received signal and produces a base-band signal. The ADC converts the base-band signal into digital data that is stored in the buffer. After a complete transmission sequence is received, the digital data may be later reassembled into the information by a digital signal processor such as a microprocessor, micro-controller, or other digital signal processing (DSP) based electronic system. Additional control circuits and procedures (not shown) are utilized to control the receiver system as will be discussed in subsequent discussions below.

According to the above excerpts, in Karr, "digital data is only processed after a complete transmission is stored in the buffer" and "the clock signals used in the signal processor can be disabled . . . during the critical reception time period." Accordingly, in the invention of Karr, the processor is disabled when data reception is occurring. In other words, in Karr, buffering of digital samples cannot occur while the processor is enabled, and processing cannot occur while buffering of digital samples is occurring. Because of this, Karr specifically teaches away from Applicant's claimed feature of "simultaneously with processing the first digital samples, buffering second digital samples." For at least this reason, Karr is not an acceptable reference for disclosing the feature that "digital samples from a receiver can be buffered while the processor is disabled." Based on the teaching away

of Karr, discussed above, one of skill in the art would not be motivated to combine Karr with the other cited references in order to arrive at Applicant's claimed invention.

Based on the above remarks, Applicant believes that the rejection of claims 1-4, 6-7, 9-15, 17, and 22 under 35 U.S.C. 103(a) has been overcome. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn, and that claims 1-4, 6-7, 9-15, 17, and 22 be allowed.

Rejection of Claim 5:

Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Sririam, Tamura, Okabayashi, Karr, and U.S. Patent No. 6,650,140 to Lee et al. (herein "Lee"). Applicant previously cancelled claim 5, and therefore this rejection is moot. Applicant respectfully requests that this rejection be withdrawn.

Rejection of Claim 16:

Claim 16 is rejected under 35 U.S.C. §103(a) as being unpatentable over Sririam, Tamura, Okabayashi, Karr and U.S. Patent Publication No. 2002/0176489 to Roohparvar (herein "Roohparvar"). Applicant previously cancelled claim 16, and therefore this rejection is moot. Applicant respectfully requests that this rejection be withdrawn.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (480) 385-5060. If necessary, the Commissioner is hereby authorized to charge payment or credit any overpayment to Deposit Account No. 50-2091 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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